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METHOD FOR SEPARATELY OPTIMIZING THIN GATE DIELECTRIC OF PMOS AND NMOS TRANSISTORS WITHIN THE SAME SEMICONDUCTOR CHIP AND DEVICE MANUFACTURED THEREBY

Abstract

A method of forming CMOS semiconductor materials with PFET and NFET areas formed on a semiconductor substrate, covered respectively with a PFET and NFET gate dielectric layers composed of silicon oxide and different degrees of nitridation thereof. Provide a silicon substrate with a PFET area and an NFET area and form PFET and NFET gate oxide layers thereover. Provide nitridation of the PFET gate oxide layer above the PFET area to form the PFET gate dielectric layer above the PFET area with a first concentration level of nitrogen atoms in the PFET gate dielectric layer above the PFET area. Provide nitridation of the NFET gate oxide layer to form the NFET gate dielectric layer above the NFET area with a different concentration level of nitrogen atoms from the first concentration level. The NFET gate dielectric layer and the PFET gate dielectric

layer can have the same thickness.